REMARKS

Claims 1-3, 5, 18-51, and 56-87 are currently pending, claims 4, 6-17, 52-55, have been canceled, and claims 18-51 and 56-66 are withdrawn. Claim 87 is new; no new matter has been added. Applicants reserve the right to pursue original and other claims in this and in other applications.

Claims 1-3, 5, 67-74, and 81-83 stand rejected under 35 U.S.C. §112, second paragraph as allegedly failing to point out and distinctly claim the subject matter which the Applicants regard as their invention. Claims 1-3, 5, 67-74, and 81-83 have been amended substantially in conformance with the Examiner's suggestions. Thus, the rejection of these claims should be withdrawn.

Claims 80-81 stand rejected under 35 U.S.C. 102 (e) as being anticipated by Kole (U.S. Pat. No. 6,501,064). Applicants respectfully traverse this rejection.

The invention is directed to measuring a breakpoint, e.g., a knee point, of a response curve representing the voltage output of an image array having an extended dynamic range. In an example of an implementation of the invention, an image sensor is provided with controllable voltage supply which provides a plurality of voltage levels to pixel in the image sensor. The image sensor also includes a reset voltage controller for controlling each pixel's reset transistor and configured to provide a full reset voltage, a partial reset voltage, and substantially no voltage.

> By flooding a light-opaque pixel with a charge and then applying an intermediate reset voltage to the pixel, the signal is read from the pixel and stored. The full reset voltage is applied to the pixel, and then the signal in the pixel is read and stored. The voltage output difference is the difference between the first and second stored signal. The voltage output difference is then used to determine the voltage of the knee point. Further, a conventional saturated pixel can be reset with an intermediate reset just prior to readout. The resulting signal can then be used to determine the voltage of the knee point.

(Abstract)

Claim 80 recites a:

> pixel comprising:
>
> > a first voltage source having an output switchable between a first and second reset supply voltage in response to a first control signal;
> >
> > a charge storage region;
> >
> > a reset transistor connected between said first voltage source and said charge storage region; and
> >
> > a control circuit for providing a gate control voltage to a gate of said reset transistor, said control circuit selectively providing a first operating control voltage and a second operating control voltage to said reset transistor, said second operating control voltage being less than said first operating control voltage and higher than a zero voltage.

Kole discloses:

> An image pick-up [that] includes a number of active sensor elements ...arranged in an array and a number of conductive lines extending over the surface of the array for the transfer of supply and signals. Each sensor element includes a light sensor (20) and an amplifier. According to the invention, a reduction in the number of lines can be achieved while functionality is maintained. In a first and a second embodiment (11; 12), a sensor element includes a first switch (S1) associated with the sensor and a second switch (S2; S3) associated with the amplifier, the switches being controlled by a common control signal. In a third embodiment (13), a sensor element includes a series arrangement of a first switch (S1) and a second switch (S2) included between the sensor and a supply line. In a fourth embodiment (14), a select signal is also used as a supply for the amplifier.

(Kole, Abstract)

Kole fails to disclose or suggest "said second operating control voltage being less than said first operating control voltage and higher than a zero voltage." Kole only teaches the reset transistor receiving either a high, inactive, and low, active, control signal. As Kole's reset transistor

is operating a switch, the control signals typically provided to the reset transistor gate to control its operation are Vth and 0 voltage levels, such that the transistor is either in an ON or OFF state. Kole's operation is different in operation from the claimed invention where "said second operating control voltage being less than said first operating control voltage and higher than a zero voltage." As such, the rejection of claim 80 should be withdrawn and the claim and its dependant claims allowed.

Claims 67, 68, and 70 stand rejected under 35 U.S.C. 103 (a) as being unpatentable over Kole in view of Merrill (U.S. Pat. Pub. No. 2002/0036700) ("Merrill"). Applicants respectfully traverse this rejection.

Claim 67 recites an:

> imaging device, comprising:
>
> a processor;
>
> an imager array coupled to said processor, one pixel of said image array comprising:
>
> a charge sharing node;
>
> a reset control circuit configured to provide a plurality of non-zero voltages;
>
> a row select transistor being switchably coupled to a first and second voltage, a gate of said row select transistor being coupled to a row select control line; and
>
> a reset transistor having source/drain regions on opposite sides of a gate, one of said source/drain regions being switchably coupled to said first and second voltage, the other of said source/drain regions being coupled to said node, a gate of reset transistor being coupled to said reset control circuit.

Kole fails to disclose "a reset control circuit configured to provide a plurality of non-zero voltages." As noted above, Kole only teaches providing an active and an inactive signal to the reset transistor gate.

Merrill is cited by the Office for allegedly teaching "a row select transistor being switchably coupled to the first and second voltage and the reset transistor and row select transistor having their own control lines."

Merrill fails to cure the deficiency of Kole and fails to disclose or suggest "a reset control circuit configured to provide a plurality of non-zero voltages." Merrill only teaches its reset transistor being controlled such that it is either active or nonactive. Thus, the rejection of claim 67 should be withdrawn and the claim allowed over the combination of Kole and Merrill.

Claims 68 and 70 depend from claim 67 and are allowable over the combination of Kole and Merrill for at least the reason noted above with respect to claim 67 and on their own merits.

Claim 69 stands rejected under 35 U.S.C. 103 (a) as being unpatentable over Kole in view of Kokubun et al. (U.S. Pat. Pub. No. 2003/0146993) in further view of Merrill. Applicants respectfully traverse this rejection.

Claim 69 depends from claim 67 and is allowable over the combination of Kole and Merrill for at least the reason noted above with respect to claim 67 and on its own merits.

Kokubun is cited by the Office for allegedly teaching a ground potential as one of a first and second voltage levels.

Kokubun fails to cure the deficiency of Kole and Merrill and fails to disclose or suggest "a reset control circuit configured to provide a plurality of non-zero voltages." Kokubun teaches away from the combination and teaches that one of voltages is a ground. Thus, the rejection of claim 69 should be withdrawn and the claim allowed over the combination of Kole and Merrill and Kokubun.

Applicants appreciate the indication that claims 75-79 and 84-86 are in condition for allowance.

New claim 87 recites:

> An image array comprising:
>
> a controllable voltage source being selectively mutually exclusively coupled to a first voltage source and a second voltage source for supplying a first and a second voltage level, respectively, said first voltage level being different from said second voltage level;
>
> a pixel comprising:
>
> a reset transistor having source/drain regions on opposite sides of a gate, one of said source/drain regions being switchably coupled to an output of said controllable voltage source, the other of said source/drain regions being coupled to an associated charge storing node;
>
> a reset control circuit coupled to a gate of said reset transistor, said reset control circuit configured to provide a first reset control signal at a first level, a second reset control signal at a second level, and a third reset control signal at a third level; where said first level is different from said second and third levels, where said second level is different from said third level.

None of Kokubun, Kole, and Merrill disclose or suggest "a reset control circuit coupled to a gate of said reset transistor, said reset control circuit configured to provide a first reset control signal at a first level, a second reset control signal at a second level, and a third reset control signal at a third level; where said first level is different from said second and third levels, where said second level is different from said third level." Thus, claim 87 should be allowable over the combination of Kole and Merrill and Kokubun.

In view of the above, Applicants believe all rejected claims in the pending application are allowable and that the application is in condition for allowance.

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Respectfully submitted,

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